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Design and Comparison of Multiplexer using Different Methodologies

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Abstract: Multiplexer can be designed using Adiabatic array logic, CMOS logic, pass transistor logic. This paper describes a multiplexer using adiabatic logic. The Adiabatic logic are low power circuits which are reversible logic to conserve energy, it brings about a great deal of power minimization in digital circuits. The proposed circuits show lesser power dissipation then the conventional static CMOS logic style. All the designs were simulated using Tanner EDA tool v15.0. Simulations were done at 90nm technologies.

Keywords: Adiabatic logic, power dissipation, power saving, Tanner EDA tool v15.0.

I. INTRODUCTION

Minimizing power consumption in high performance and handled devices has become a major challenge in the design of modern electronic system. In recent years a variety of techniques and technologies have been developed including the use of near- threshold and sub-threshold logic. Adiabatic or reversible logic techniques have also been considered an attractive low power alternative to standard CMOS logic circuits [1].

The term Adiabatic is taken from Greek that means "impassable" and frequently used in thermodynamics, which means that there is no loss or gain of energy in the form of heat in the system [2] . Adiabatic logic operates with an AC power supply and it works with the concept of switching which is used to reduce energy dissipated by resistive heating of components and by allowing charge recovery [1]. The term adiabatic logic is used in low power VLSI circuits which implements reversible logic. There are several important principles that are shared by all low power adiabatic systems. It includes only turning switches on where there is no potential difference between them, only turning switches off when no current flows through them. The power supplies of adiabatic logic circuits have also used circuit element capable of storing energy this is often done using inductors, which store the energy by converting it to magnetic flux [2].

In recent years a number of adiabatic logic families have been developed including efficient charge recovery logic (ECRL), positive feedback adiabatic logic (PFAL), two phase adiabatic static clocked logic (2PASCL), 2N2N2P logic, proposed adiabatic logic etc [6].

Multiplexer is the type of electronic device which is used to select various analog or digital input signals and allows them to select input into a single line. A multiplexer has 2n inputs where, 'n' select lines which are used to select which input line to send to the output. Multiplexer will be used in increasing the amount of data which can be sent over the network within a definite amount of time and bandwidth. A multiplexer is also called as a data selector.

Multiplexer is also used in implementing Boolean function of multiple variables. Power can be reduced either architecture level or module level or circuit level. Multiplexer is a special type of combinational circuit which selects only one of 'n' given data inputs and routs it to the output [2].

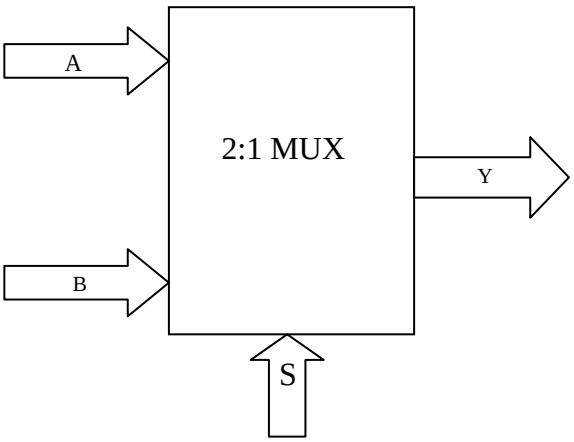

Fig. 1 Symbol of 2:1 MUX

II. PREVIOUS WORK

Power can be reduced either architecture level or module level or circuit level. Previously, various versions of multiplexer have been made with the help of CMOS logic, pass transistor logic, and adiabatic logic. But, CMOS logic consumes high power and has more complexity in the circuit. In Pass transistor logic complexity of the circuit is less than the CMOS logic. Transistor requires both NMOS and PMOS in different well, transistor is in saturation region during charging process where as transistor is always in non-saturation region during discharging process.

Previous work in Multiplexer based adiabatic logic involve the usage of NMOS pull down configuration,

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cross coupled inverter, two phase drive adiabatic dynamic CMOS logic (2PADCL). Total power consumption of the multiplexer is more. This paper analyses the total power consumption of the multiplexer circuit using the standard logic style and proposes a new logic style with lesser power consumption.

III. CIRCUIT DESIGN OF MULTIPLEXER

Multiplexer is a combinational circuit which select only one of 'n' given data inputs and routes it to the output. The selection of one of the inputs is done by 'm' select inputs, with 2m = n.
The block diagram of 2:1 multiplexer is shown in fig. 1. Its truth table is given in table 1.

TABLE I Truth Table of 2:1 MUX

S	Y
1	A
0	B

A. PASS Transistor based Multiplexer
Pass transistor has various techniques, but in this paper we have used GDI technique. GDI technique is an area efficient technique which takes less power consumption by reducing the number of transistors. GDI technique needs to use twin well process or silicon on insulator for chip composition. Twin well process gives separate optimization of p-type and n-type transistor and also optimizes gain and VTH of p-type and n-type device. GDI technique provides an extra input for the cell and maintains the circuit complexity.

GDI technique solves the problem of poor ON to OFF transition characteristic of PMOS and providing the full swing at internal node of circuit. Fig.2 show the 2 is to 1 MUX select line S is common input for gate terminal of PMOS_1 and NMOS_1. Input A and input B is connected to the source terminal of PMOS_1 and NMOS_1 respectively. When S is low then PMOS_1 is ON and pass the input B from source terminal to drain terminal. When S is high then NMOS_1 is ON and PMOS_1 is off. Output is common for drain terminal for PMOS_1 and NMOS_1.

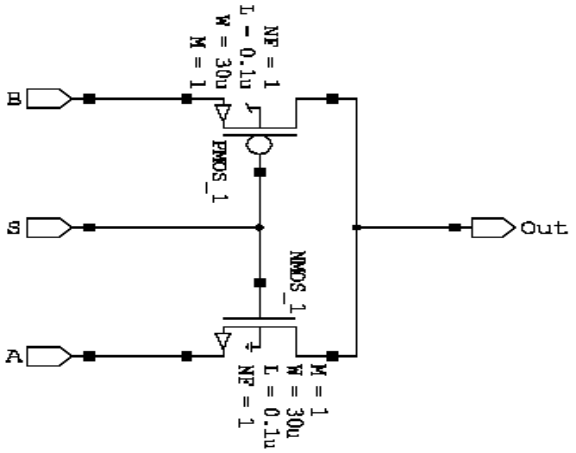

Fig.2. Pass transistor (GDI) based Multiplexer

B. CMOS based Multiplexer
CMOS logic technique is used for design of Multiplexer. In CMOS circuit power dissipation is occur at switching of the device. In CMOS circuit two types of power dissipation occurs. First is dynamic power and second is static power. Fig.3 depicts the CMOS based 2 is to 1 multiplexer, select line S is common input for both AND gate. Input A and input B is connected to the AND_1 gate and AND_2 gate respectively. When S is low input B is pass, when S is high input A is pass through the Output.

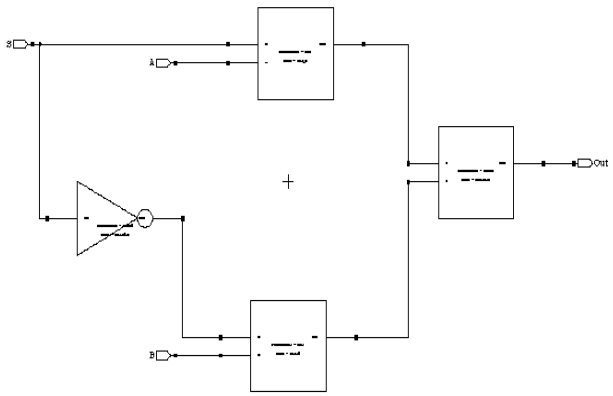

Fig.3. CMOS logic based Multiplexer

C. Adiabatic Array Logic based Multiplexer
The adiabatic array logic has an array of transmission gate to form an AND-plane and a wired OR-plane forms the second plane. On the basis of array logic the circuit drives a sinusoidal power supply. The adiabatic gate is operating as parallel transmission gate chains. Fig.4 depicts Adiabatic Array logic based Multiplexer, which is design using tanner EDA tool V15.0. Simulation were done at 90nm technology, with W/L = 0.1µm/0.1µm for both PMOS and NMOS. V_{PCLK} = 1.8v (peak to peak), and load capacitance 0.005pf. The design employs four terminal MOSFETs whose substrate is connected to VDD and GND for PMOS and NMOS respectively.

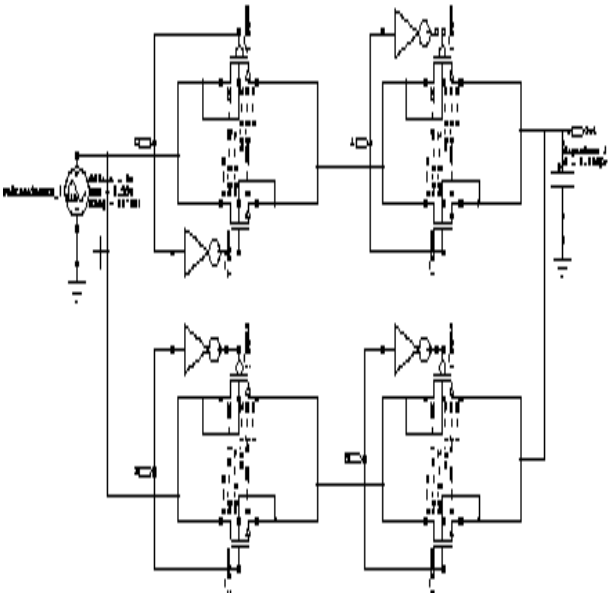

Fig.4. Adiabatic Array Logic based Multiplexer

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IV. SIMULATION AND RESULT

All design is to be simulated using tanner EDA tool V15.0. Simulations are done at 90nm technology. Fig.5 shows the waveform of Pass Transistor based Multiplexer at input combination '0011' and '0011'.

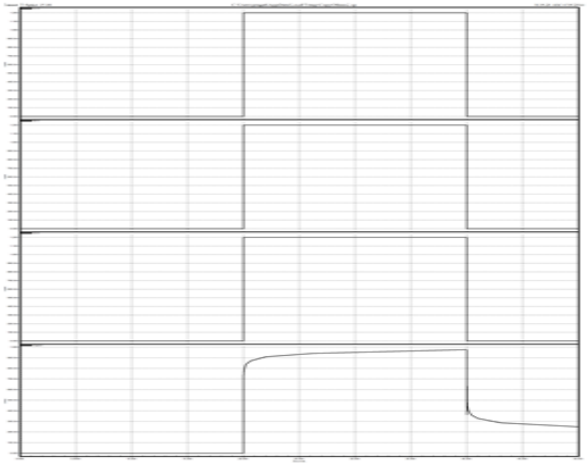

Fig.5. Waveform of Pass transistor based Multiplexer

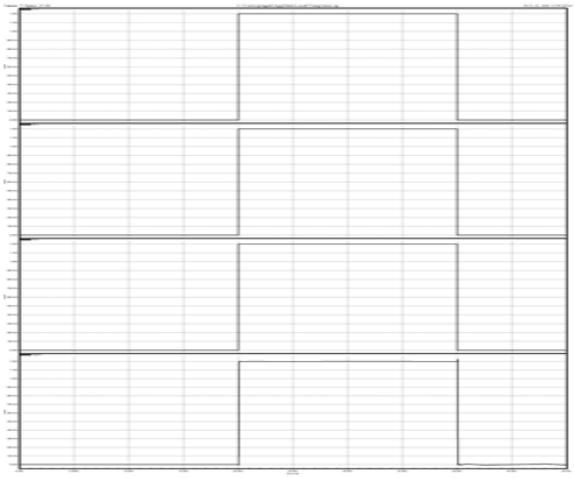

Fig.6. Waveform of CMOS based Multiplexer

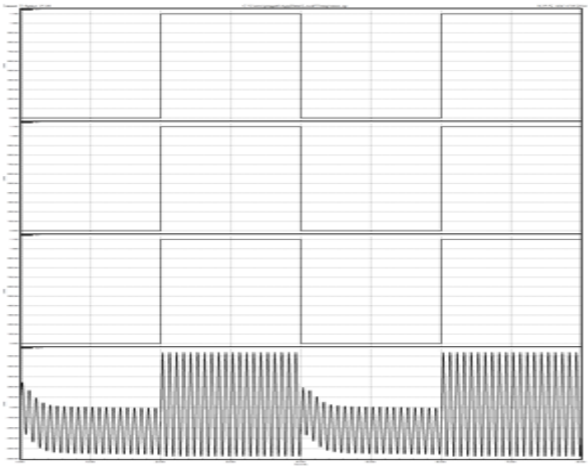

Fig.7. Waveform of Adiabatic Array logic based Multiplexer

Fig.6 shows the waveform of CMOS logic based Multiplexer. In this when select line S is low input B is pass through the output, and when select line S is high input A is pass through the output. Fig. 7 shows the waveform of Adiabatic array logic based Multiplexer. In this all input is connected to PMOS and NMOS combination.

TABLE II Performance analysis of various logic styles for Multiplexer

S.NO.	LOGIC	POWER CONSUMPTION (µm)
1.	Pass Transistor based Multiplexer	2.95
2.	CMOS based Multiplexer	7.98
3.	Adiabatic Array Logic based Multiplexer	2.20

V. CONCLUSION

The main aim behind the whole works is to design and propose new low power digital circuits for the Multiplexer employing the Adiabatic Array Logic. The AAL family is chosen for the work as a systematic and simple approach for Boolean expressions with multiple terms. The proposed circuit consumes only about a quarter amount of power in comparison to the conventional CMOS in this converter. 72.43% decreases power consumption of AAL with respect to CMOS logic. Whereas, 25.42% decreases power consumption of AAL with respect to Pass transistor.

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